A1 cancel

30. (New) The array according to claim 29, wherein said horizontally stacked pseudo-TFT transfer gate is formed on a p+ silicon layer utilizing a lateral overgrowth epi technique via a single crystal seed area.

Please amend the following claims:

A2 to be hereinafter

12. (Amended) An array of planar T-RAM cells comprising:

a plurality of T-RAM cells, said plurality of T-RAM cells being arranged in an array and fabricated over a substrate, each of said plurality of T-RAM cells including a first and a second device, said first device being buried underneath said second device, wherein said second device covers the entire top surface of said first device, and further wherein the top surface of said second device forms a planar top surface of each said T-RAM cell.

13. (Amended) The array according to Claim 12, wherein said first device is a buried vertical thyristor and said second device is a horizontal transfer gate.

15. (Amended) The array according to Claim 12, wherein said substrate is a semiconductor SOI or bulk wafer.

16. (Amended) The array according to Claim 13, wherein a base of said thyristor

A3 is surrounded by a surrounded gate.

17. (Amended) The array according to Claim 12, wherein said planar top surface of each T-RAM cell provides for simplified fabrication of metal wirings, said wirings being fabricated over said planar top surface of said T-RAM cells, said wirings for interconnecting